Customer Training Workshop
Traveo™ II I/O System

Q2 2021

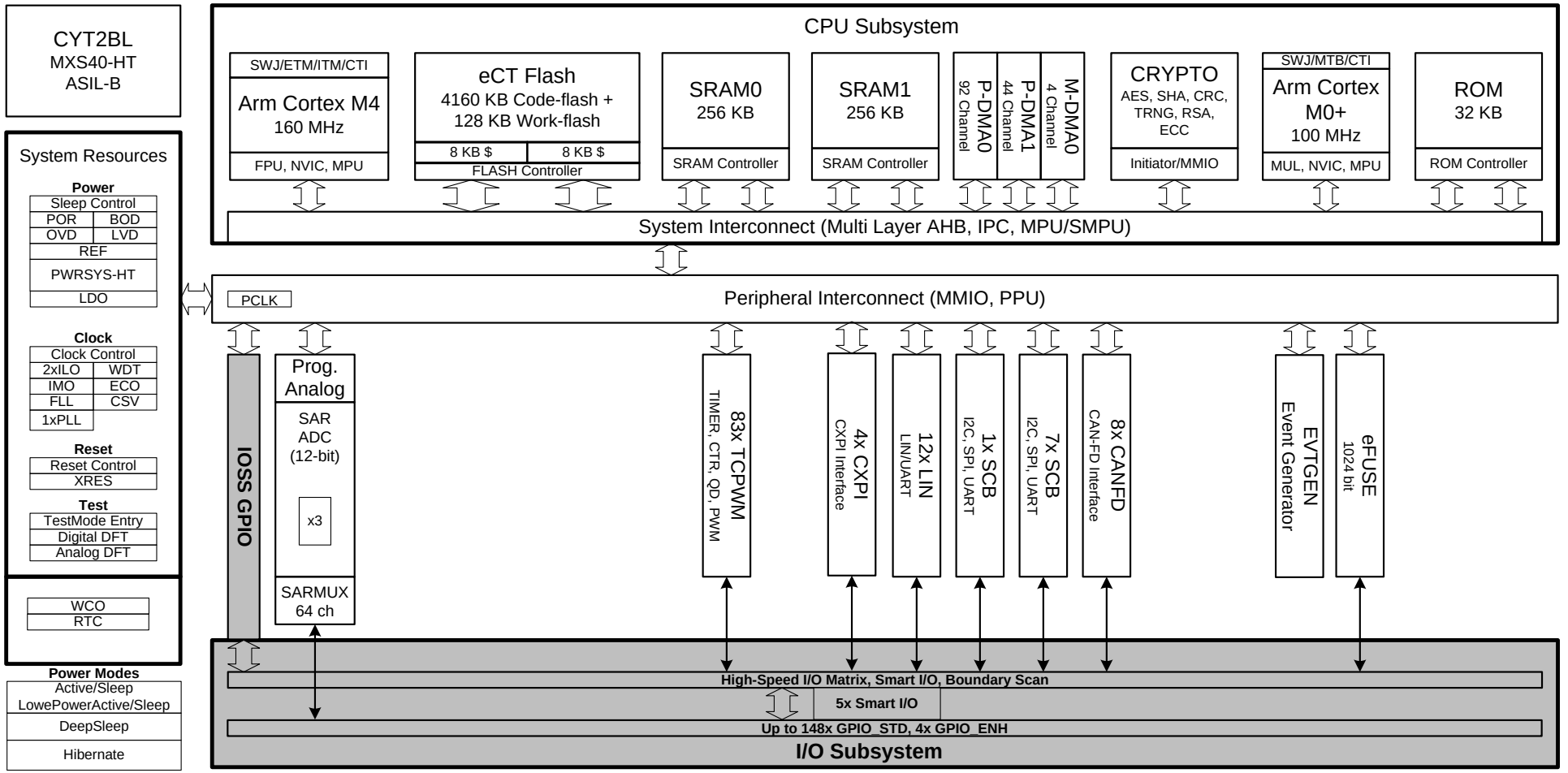
Target Products

› Target product list for this training material

Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Body Controller Entry	CYT2B6	Up to 576 KB
Traveo II Automotive Body Controller Entry	CYT2B7	Up to 1088 KB
Traveo II Automotive Body Controller Entry	CYT2B9	Up to 2112 KB
Traveo II Automotive Body Controller Entry	CYT2BL	Up to 4160 KB
Traveo II Automotive Body Controller High	CYT3BB/CYT4BB	Up to 4160 KB
Traveo II Automotive Body Controller High	CYT4BF	Up to 8384 KB
Traveo II Automotive Cluster	CYT3DL	Up to 4160 KB
Traveo II Automotive Cluster	CYT4DN	Up to 6336 KB

Introduction to Traveo II Body Controller Entry

› The I/O System includes GPIO, HSIOM, and Smart I/O functions

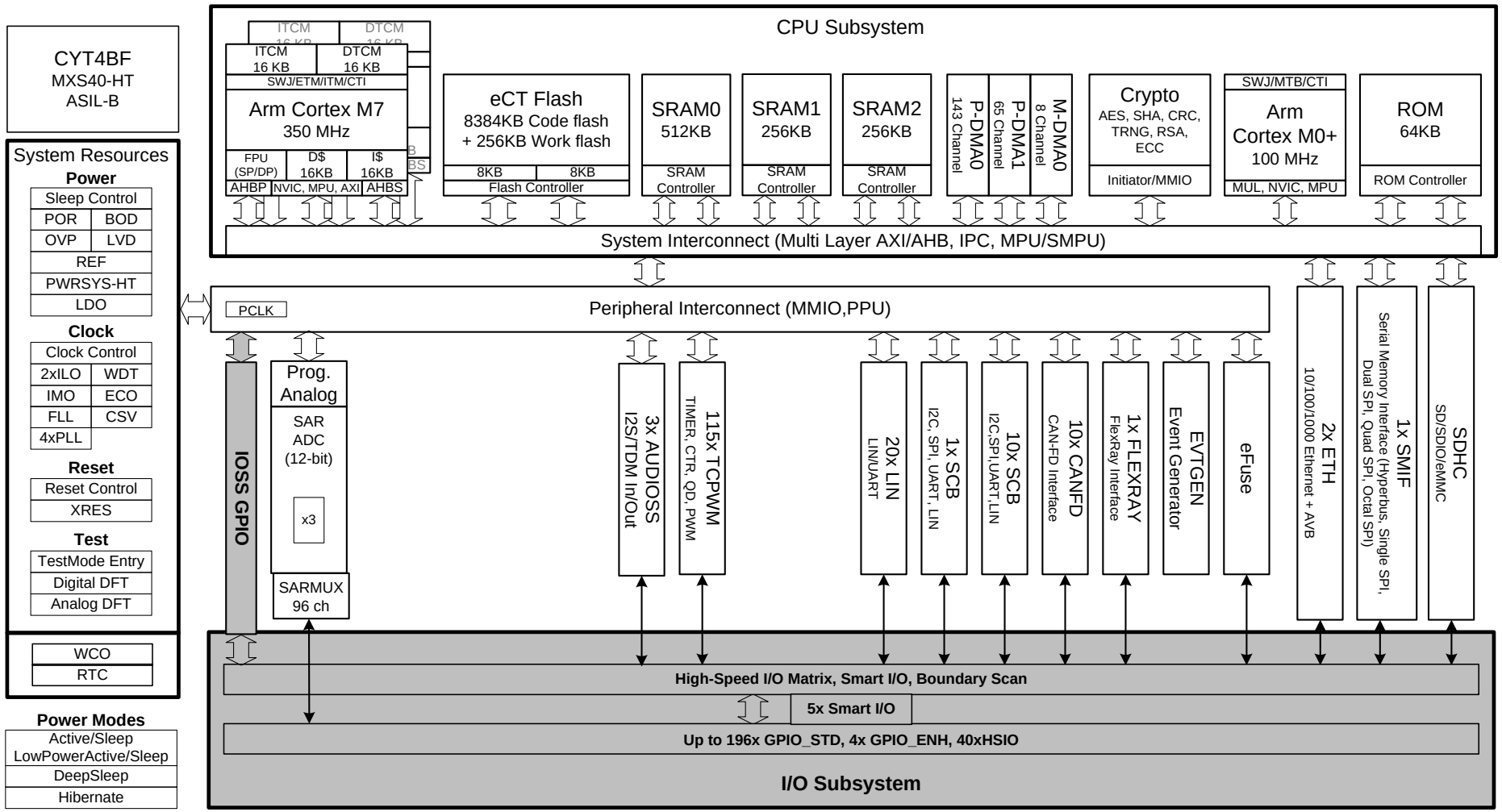


Hint Bar

Review TRM chapter 22 for additional details

Introduction to Traveo II Body Controller High

› The I/O System includes GPIO, HSIOM, and Smart I/O functions

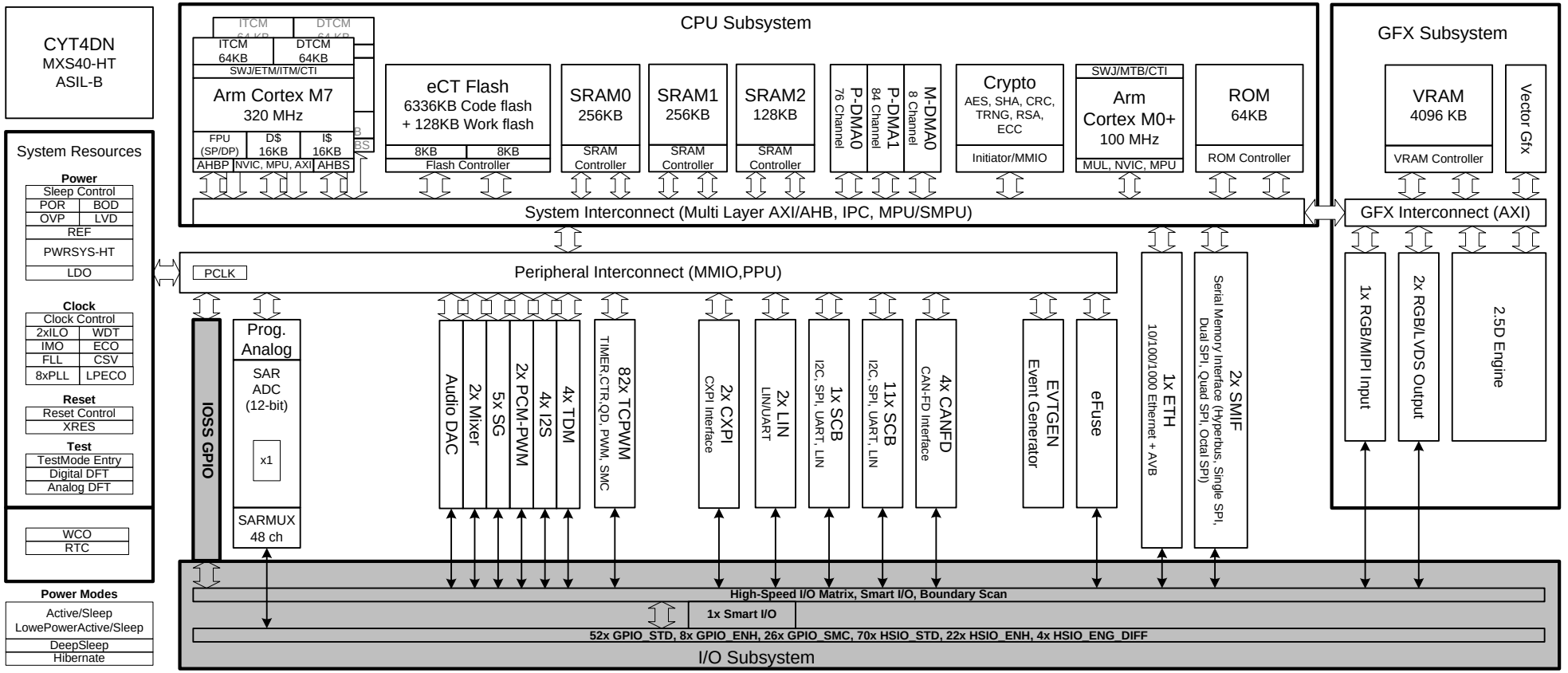


Hint Bar

Review TRM chapter 22 for additional details

Introduction to Traveo II Cluster

› The I/O System includes GPIO, HSIOM, and Smart I/O functions



Hint Bar

Review TRM chapter 22 for additional details

I/O System Overview

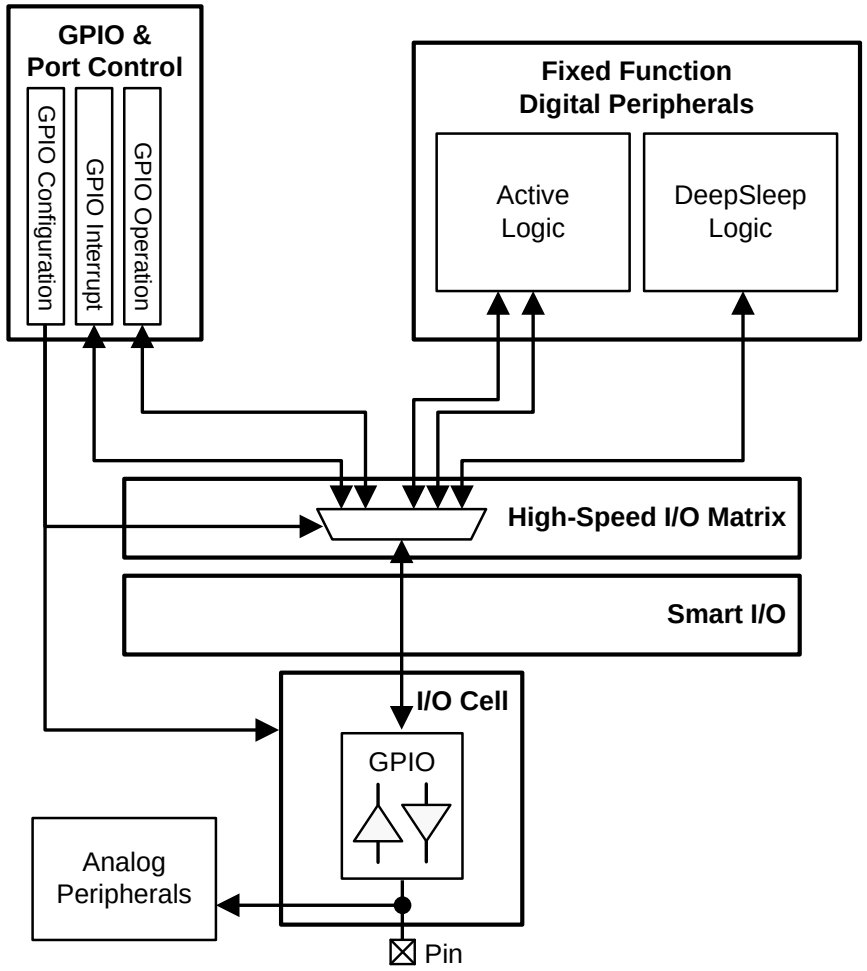
- Interface between CPU and peripheral components to the outside world
- Features
  - Analog and digital input and output capabilities
  - Eight drive modes
  - Slew rate control
  - High-speed I/O Matrix (HSIOM)
  - Edge-triggered interrupts on all GPIOs
  - Hold I/O state in DeepSleep mode
  - Smart I/O™

Hint Bar

Review TRM section 22.1 for additional details.

I/O System Block Diagram

› I/O System Components

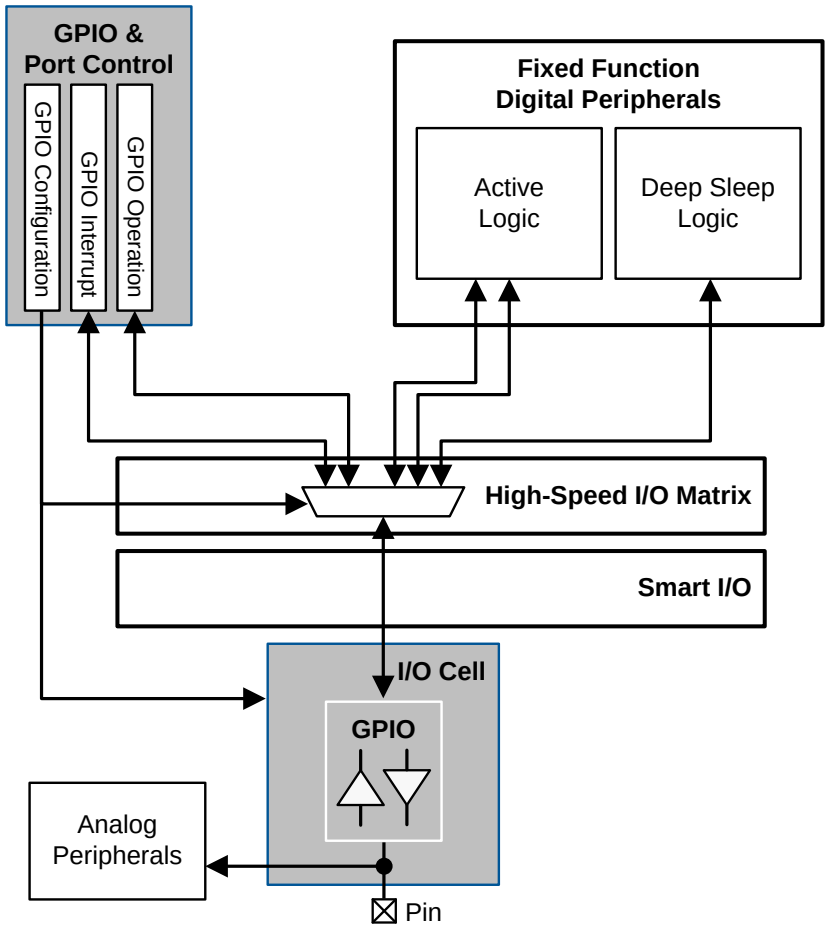


Hint Bar

Review TRM section 22.2 for additional details.

I/O System Components

- GPIO and Port Control I/O cell
  - Digital input
  - +B input support
  - Digital output drive modes
  - Slew rate control
  - GPIO SMC
  - High-speed I/O
  - Interrupt
  - Behavior in low-power modes



Hint Bar

Review TRM section 22.2 for additional details.

Digital Input

- Each pin's input buffer trip point is configurable for the following modes:
  - CMOS (Default)
    - VIH: 0.7 × VDDIO
    - VIL: 0.3 × VDDIO
  - TTL
    - VIH: 2.0 V
    - VIL: 0.8 V
  - Automotive
    - V_{IH}: 0.8 × V_{DDIO}
    - V_{IL}: 0.5 × V_{DDIO}

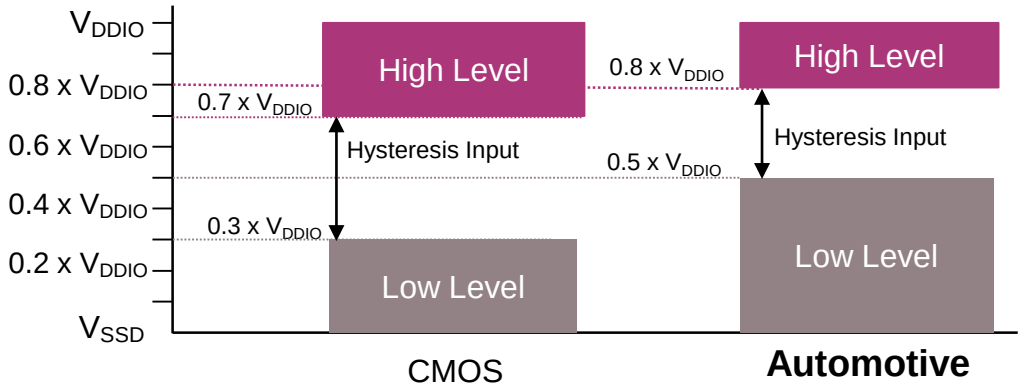
Hint Bar

Review TRM section 22.5 for additional details.

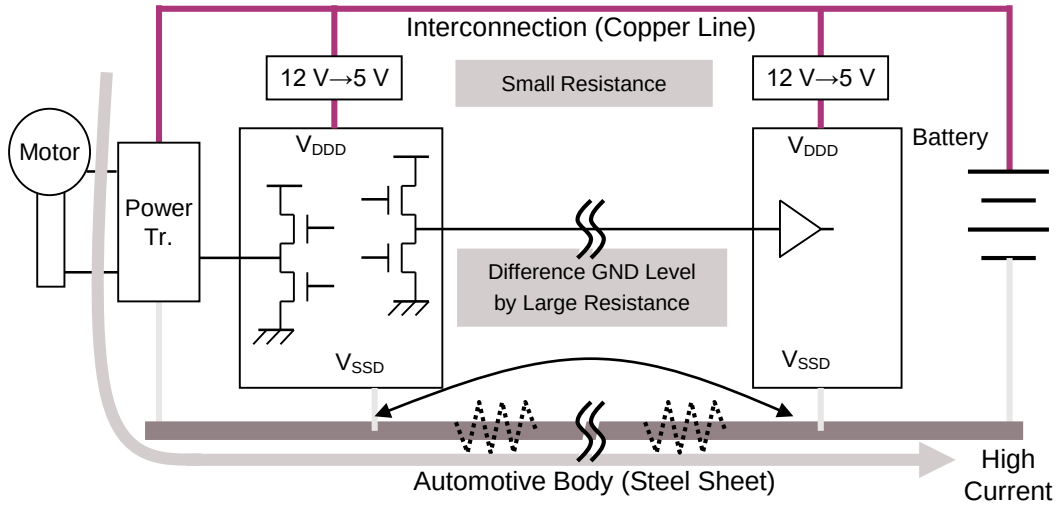
Use Case for Automotive Trip Point

› Supports higher threshold input for GND variation that occurs due to high current in the electronic control unit (ECU)

Input Spec

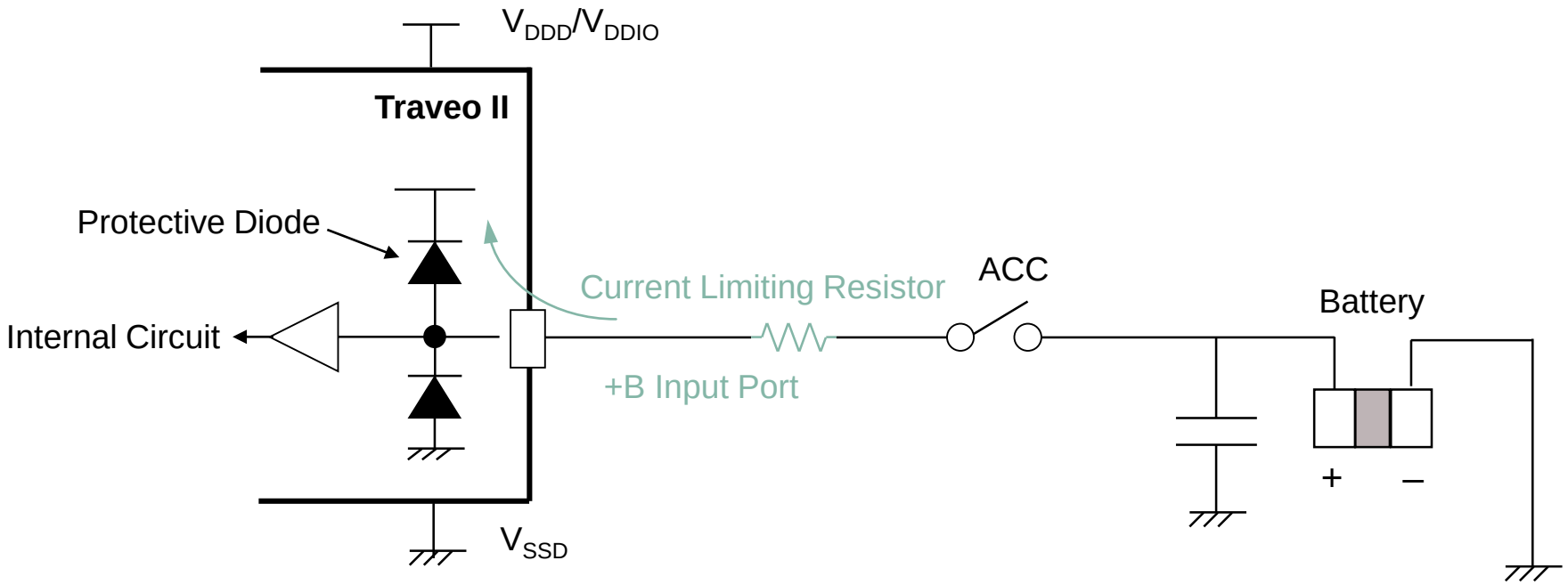


Use Case



+B Input Support

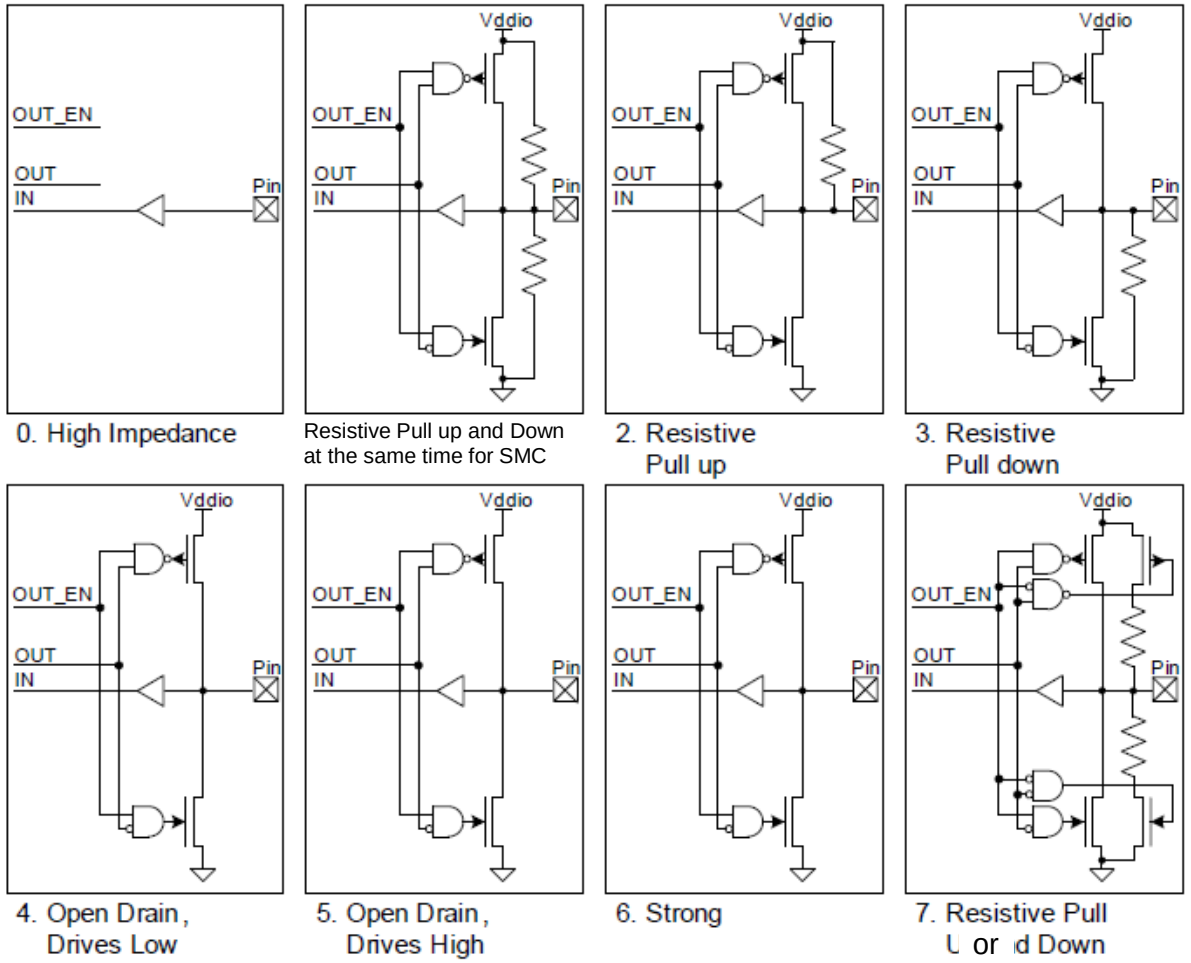
- Supports +B input to GPIO by adding the current limiting resistor
- Reduces the external parts and PCB footprint



Hint Bar

Review the specific device datasheet for additional details

Digital Output Drive Modes



Each I/O is individually configurable to one of eight drive modes by software[1]

Use Case

0. Analog/digital input/unused
1. Resistive pull up and down at the same time for SMC
2-3. Interface with open drain drive lines
4. Signal is externally pulled up (e.g., I^2C)
5. Signal is externally pulled down
6. Digital output signal or drive external devices
7. Be driven by other signals

Hint Bar

Review TRM section 22.6.1 for additional details

[1] See the Register TRM (GPIO_PRTx_CFG) for additional details.

GPIO_STD/ENH Drive Strength

› Drive strength can be set to one of four levels

Spec	Strength (DRIVE_SEL)	V_{DDIO} or V_{DDD}		Conditions	
		2.7 V to 4.5 V	4.5 V to 5.5 V		
IOL	0, 1	2 mA	5 mA (6 mA)	GPIO_STD	V_{OL} = 400 mV (600 mV)
		2 mA	5 mA	GPIO_ENH	V_{OL} = 400 mV
		6 mA		GPIO_ENH	V_{OL} = 600 mV
	2	1 mA	2 mA	GPIO_STD, GPIO_ENH	V_{OL} = 400 mV
	3	0.5 mA	1 mA	GPIO_STD, GPIO_ENH	V_{OL} = 400 mV
IOH	0, 1	-2 mA	-5 mA	GPIO_STD, GPIO_ENH	V_{OH} = (V_{DDIO} or V_{DDD}) – 500 mV
	2	-1 mA	-2 mA	GPIO_STD, GPIO_ENH	V_{OH} = (V_{DDIO} or V_{DDD}) – 500 mV
	3	-0.5 mA	-1 mA	GPIO_STD, GPIO_ENH	V_{OH} = (V_{DDIO} or V_{DDD}) – 500 mV

Hint Bar

Review the datasheet and TRM section 22.6.2 for additional details

GPIO_STD/ENH Slew Rate Control

- Programmable output driver configuration for some GPIO pins[1]
  - Fast Slew rate
    - Full drive strength: 0, 1
    - 1/2 drive strength: 2
    - 1/4 drive strength: 3
  - Slow Slew rate (GPIO_ENH only)
    - Full drive strength: 0

Spec	Slew Rate Mode	Min	Max	Conditions
Tr/Tf	Fast, Strength = 0 (GPIO_STD, GPIO_ENH)	1 ns	10 ns	10%/90% 20-pF load
	Slow, Strength = 0 (GPIO_ENH)	20 ns x (V_{DDD}/5.5)	160 ns	

- Advantage
  - Slower slew rate can reduce EMI and crosstalk
- Use Case
  - Slower slew rate is used for low-frequency signals or signals without strict timing constraints

Hint Bar

Review the datasheet and TRM section 22.6.2 for additional details

[1] See the Register TRM (GPIO_PRTx_CFG_OUT) for additional details. Slew Rate Control is not available on all GPIO ports.

GPIO SMC (GPIO_SMC)[1]

- Supports significant drive strength than GPIO_STD and GPIO_ENH
  - For Stepper Motor Control (SMC)
    - 30-mA drive, 25 °C < TA ≤ 105 °C
    - 40-mA drive, –30 °C < TA ≤ 25 °C
    - 50-mA drive, –40 °C ≤ TA ≤ 30 °C
- Drive Select[2]

DRIVE_SEL[0:1]	SLOW (Slew Rate Control)	Drive Strength at 4.5 V
00	0	5 mA
00	1	30 mA
01	0/1	5 mA
10	0/1	2 mA
11	0/1	1 mA

Hint Bar

Review the datasheet for additional details

[1] Not all devices support GPIO_SMC functionality. Refer to the specific device datasheet for availability of GPIO_SMC.
[2] This table consists only parameter target values for orientation. The device specification is only mentioned in the appropriate device datasheet.

High-Speed I/O Standard (HSIO_STD)[1]

- Supports 3.3 V High-Speed Interfaces
  - Serial Memory Interface
    - Single, Dual, Quad, or Octal Serial Peripheral Interface (SPI)
    - HyperBus
  - Secure Digital Host Controller (SDHC) Interface
    - Secure Digital (SD) cards
    - Secure Digital Input Output (SDIO) cards
    - Embedded Multimedia Card (eMMC) based memory devices
  - Ethernet
    - Media Independent Interface (MII)
    - Reduced Media Independent Interface (RMII)
    - Gigabit Media Independent Interface (GMII)
    - Reduced Gigabit Media Independent Interface (RGMII)
- Drive Select

DRIVE_SEL[0:1]	Description
00	HSIO default mode
01	GPIO Full drive strength
10	GPIO 1/2 drive strength
11	GPIO 1/4 drive strength

Hint Bar

Review the datasheet and TRM section 22.4 for additional details

HSIO_STD does not support:

- Slew rate control

- DeepSleep operation

- Analog connections

[1] Not all devices support HSIO_STD functionality. Refer to the specific device datasheet for availability of HSIO_STD and the specification of each drive strength.

High-Speed I/O Standard Low Noise (HSIO_STD_LN)[1]

- Supports clocking and signaling up to 133 MHz for BGA packages and 100 MHz for TEQFP packages
- Supports High-Speed Interfaces
  - Graphics Input / Output
  - Ethernet and Serial Memory Interface
- Drive Select[2]

DRIVE_SEL_EXT[0:2]	Mode Supported	Slew Rate Control	Slew Rate (V/ns)	Voltage Range	Frequency (MHz)	Load (pF)
000	xSPI-266	0	1.37	3.0 V to 3.6 V	133	15
		1	1.25	3.0 V to 3.6 V	125	15
001	xSPI-200	0	1.03	3.0 V to 3.6 V	100	15
		1	0.9	3.0 V to 3.6 V	90	15
010	Graphics	0	0.43	3.0 V to 3.6 V	80	15
		1	0.3	3.0 V to 3.6 V	60	15
111	Graphics 64 MHz Ethernet 50 MHz	0	0.31	3.0 V to 3.6 V	64	15
		1	0.24	3.0 V to 3.6 V	50	15
		0/1	0.43	4.5 V to 5.5 V	80	15
100	SPI 12 MHz GPIO support	0/1	0.11	3.0 V to 3.6 V	12	20
		0/1	0.15	4.5 V to 5.5 V	20	20
101, 110, 111	Unused	N/A	N/A	N/A	N/A	N/A

Hint Bar

Review the datasheet and TRM section 22.6 for additional details

[1] Not all devices support HSIO_STD_LN functionality. Refer to the specific device datasheet for availability of HSIO_STD_LN.
[2] This table consists only parameter target values for orientation. The device specification is only mentioned in the appropriate device datasheet.

High-Speed I/O Enhanced

- Supports High-Speed Interfaces
  - High-Speed I/O Enhanced (HSIO_ENH)[1]
    - Supports signaling up to 200 MHz for High-Speed Interface
      - xSPI400(1.8V), xSPI333(3.3V), xSPI266(3.3V)
  - High-Speed I/O Enhanced Differential (HSIO_ENH_PDIFF)[1]
    - Supports clocking up to 200 MHz, to output clocks (normal and inverted)
- Drive Select[2]

DS_TRIM[0:2]	Description	Voltage Support	Mode Supported	Package Support	Memory Support
000	Default (50 Ω)	N/A	N/A	N/A	N/A
001	120 Ω	3.3 V	xSPI-266	TQFP	Single
010	90 Ω	N/A	N/A	N/A	N/A
011	60 Ω	3.3 V	xSPI-266	TQFP	Dual
100	50 Ω	1.8 V	xSPI-400	BGA	Single
101	30 Ω	3.3 V	xSPI-333	BGA	Single
110	20 Ω	1.8 V	xSPI-400	BGA	Dual
111	15 Ω	3.3 V	xSPI-333	BGA	Single

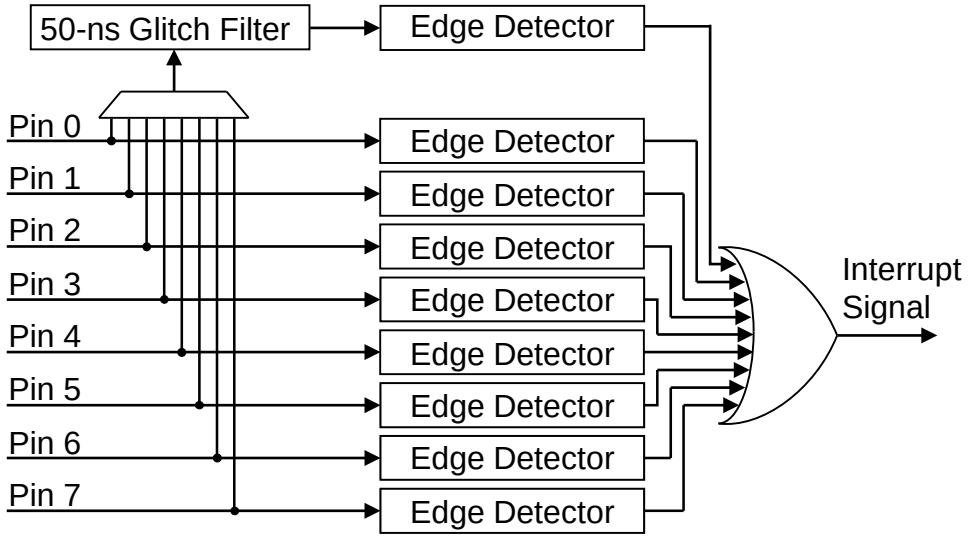
Hint Bar

Review the datasheet and TRM section 22.6 for additional details

[1] Not all devices support HSIO_ENH and HSIO_ENH_PDIFF functionality. Refer to the specific device datasheet for availability of HSIO_ENH and HSIO_ENH_PDIFF.
[2] This table consists only parameter target values for orientation. The device specification is only mentioned in the appropriate device datasheet.

GPIO Interrupt

- All port pins can generate GPIO interrupts and status registers[1]
- GPIO interrupt signal is generated by one per port
- Edge detector supports rising, falling, and both edges in all power modes[2]
- Glitch filter can be used by one pin per port[3]



- Use case
  - Wakeup interrupt from low-power mode (e.g., CAN wakeup)
  - Detect the input signal state change (e.g., switch)

Hint Bar

Review TRM section 22.10 for additional details

[1] See the Register TRM (GPIO_PRTx_INTR) for additional details.
[2] See the Register TRM (GPIO_PRTx_INTR_CFG) for additional details.
[3] If more longer pulse suppression width is necessary, use Smart I/Os.

Behavior in Each State

State	Status
Reset	› All GPIOs are in high-impedance analog state and the input buffers are disabled
Sleep	› GPIO pins are active › Can be driven by most peripherals, such as TCPWM and SCB › Any GPIO can be used to wake the device
DeepSleep	› GPIO pins connected to the DeepSleep domain peripheral (SCB[0]) are functional › All other pins are hold/frozen and will maintain the last output driver state and I/O configuration › GPIO interrupts are functional on all I/Os and can be used to wake the device
Hibernate	› Only select I/Os can be used to wake the device[1] › All other pins are on hold/frozen and will maintain the last output driver state and I/O configuration

Hint Bar

Review TRM section 22.9 for additional details

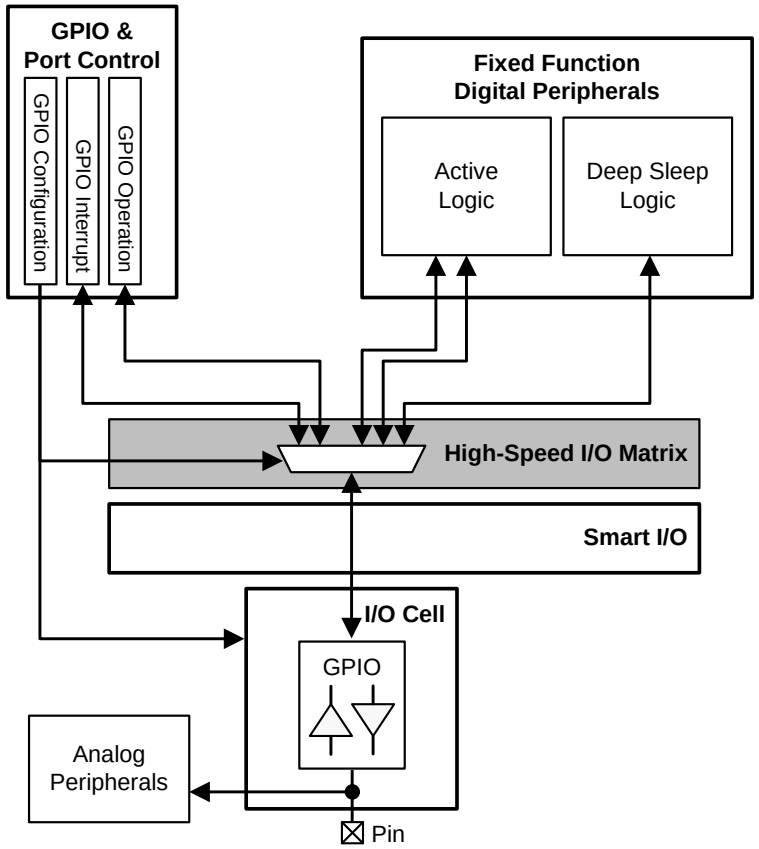
Review the Device Power Modes training section for details on the device power modes

- Advantages
  - Reduces power consumption while keeping the last I/O driver state
  - Any I/O can be used as wakeup interrupt except in Hibernate mode

[1] Traveo II body family supports up to two GPIO interrupts, whereas Traveo II cluster family supports up to four GPIO interrupts

I/O System Block Diagram - HSIOM

- High-Speed I/O Matrix
  - Routing internal CPU and peripheral signals to and from GPIOs



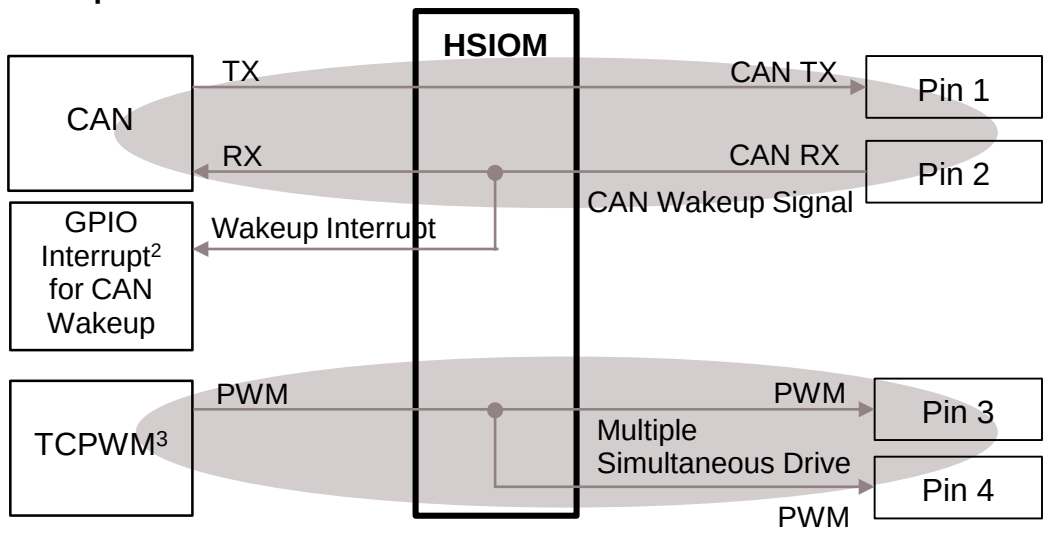
Hint Bar

Review TRM section 22.7 for additional details

[1] Traveo II body family supports up to two GPIO interrupts, whereas Traveo II cluster family supports up to four GPIO interrupts

High-Speed I/O Matrix (HSIOM)

- Routing internal peripheral signals to and from GPIOs
- GPIOs can be shared with multiple functions
- Multiplexes the pin connection to a user-selected peripheral[1]
- GPIO interrupt has no dependency on HSIOM configuration[2]
- Use Case:
  - CAN Wakeup
  - Multiple simultaneous drive by PWM output[3]



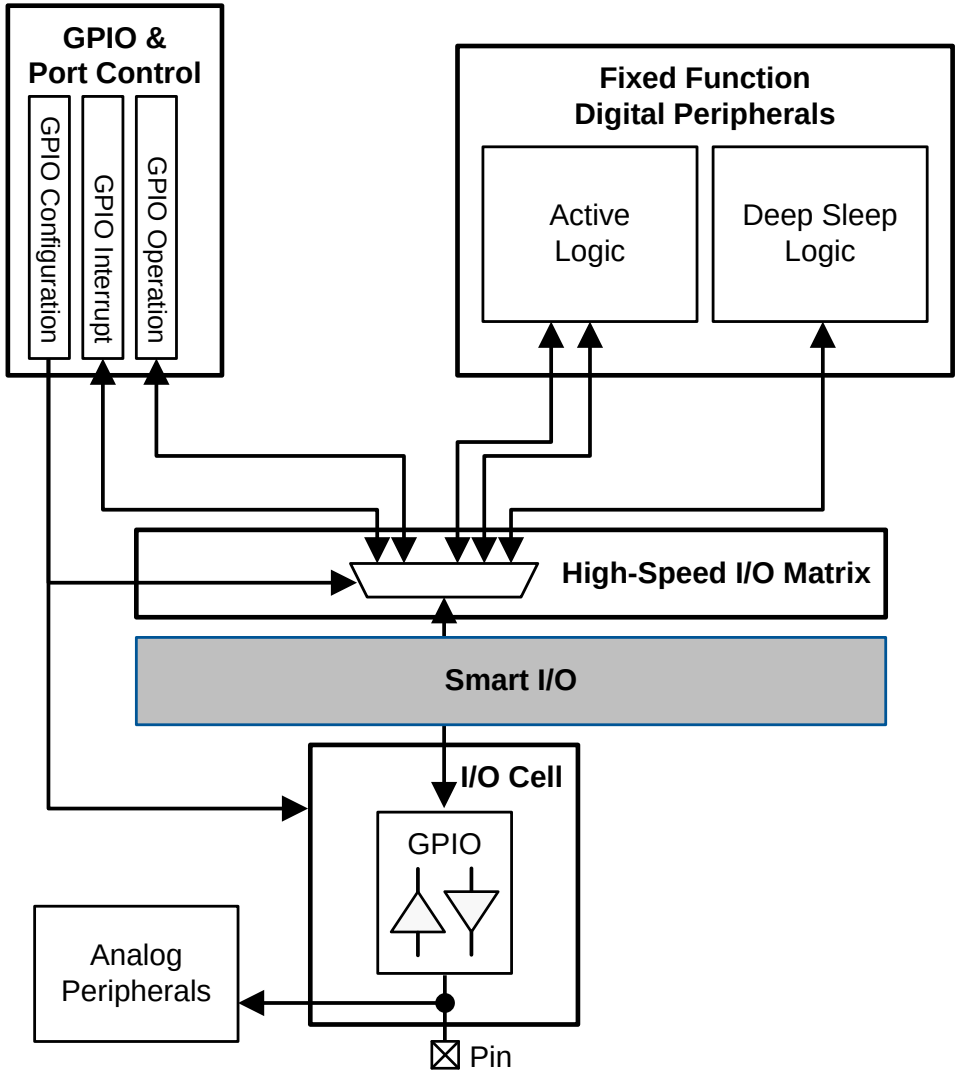
Hint Bar

Review the datasheet and TRM chapter 22.7 for additional details

[1] See the Register TRM (HSIOM_PORT_SELx) for additional details.
[2] Do not change the HSIOM configuration before going to low power mode.
[3] It depends on the pin assignment. For details on pin assignment, refer to the device datasheet.

I/O System Block Diagram – Smart I/O

- Smart I/O
  - Smart I/O signal paths
  - Block components
  - Routing

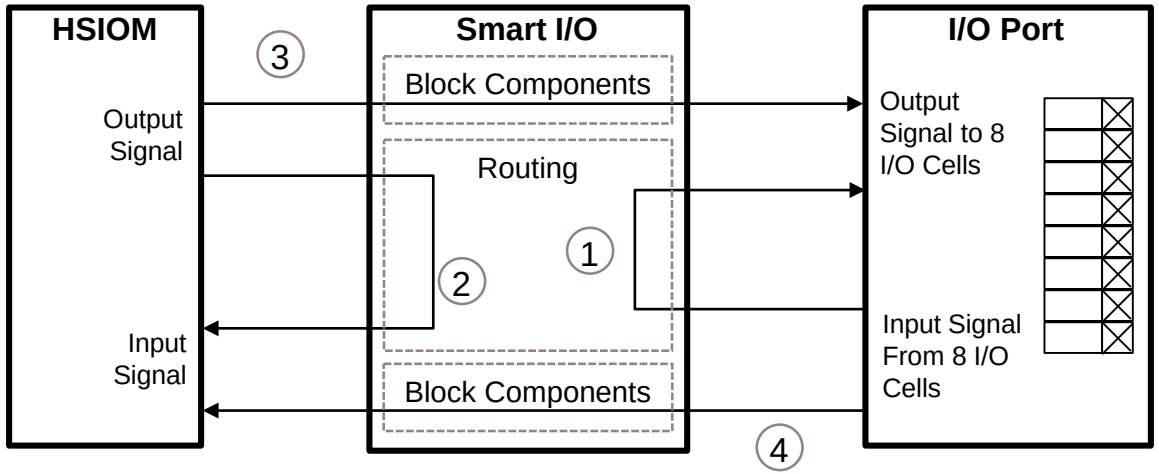


Hint Bar

Review TRM section 22.12 for additional details

Smart I/O Signal Paths

1. Observe input signals directly and control output signals directly
2. Operate on and modify HSIOM output signals and route the modified signals to HSIOM input signals
3. Operate on and modify HSIOM output signals and route the modified signals to output signals
4. Operate on and modify input signals and route the modified signals to HSIOM input signals



- Use cases
  1. Simple logic control without CPU involvement
  2. Communication peripheral loopback test
  3. Inverting SPI output signal polarity
  4. Inverting SPI input signal polarity or as a glitch filter for the input signal

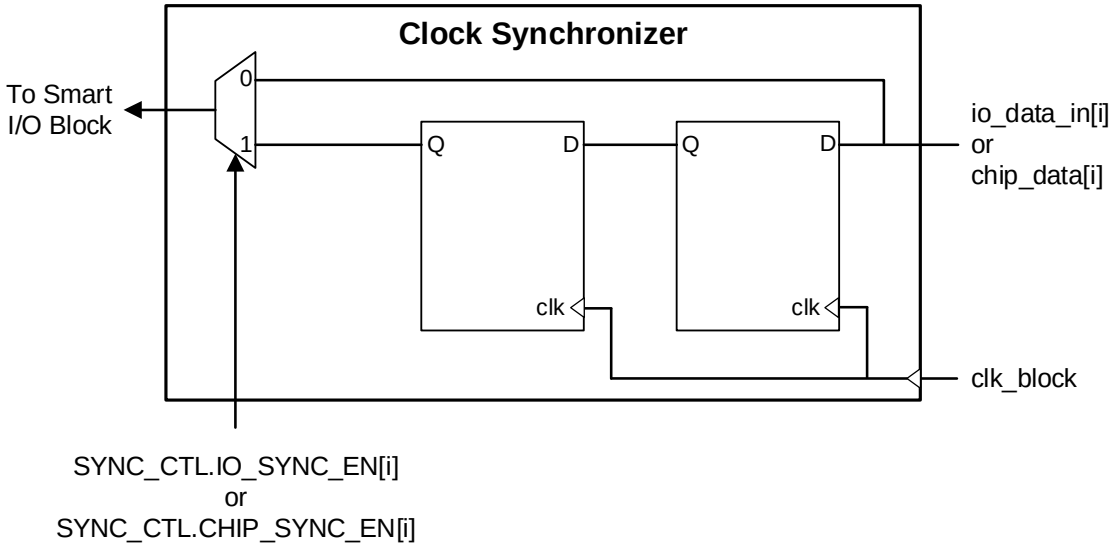
Hint Bar

Review TRM section 22.12 for additional details

Refer to Block Components and Routing for additional details

Block Components (1/2)

- Internal Smart I/O logic components
  - Clock and reset
    - Used for all components
  - Data unit
    - Consists of a simple 8-bit data path
- Synchronizers
- Each GPIO input signal and device input signal (HSIOM input) can be used either asynchronously or synchronously
  - To use the signals synchronously, a double flip-flop synchronizer is placed on both the signal paths to synchronize the signal to the Smart I/O clock (clk_block)



Hint Bar

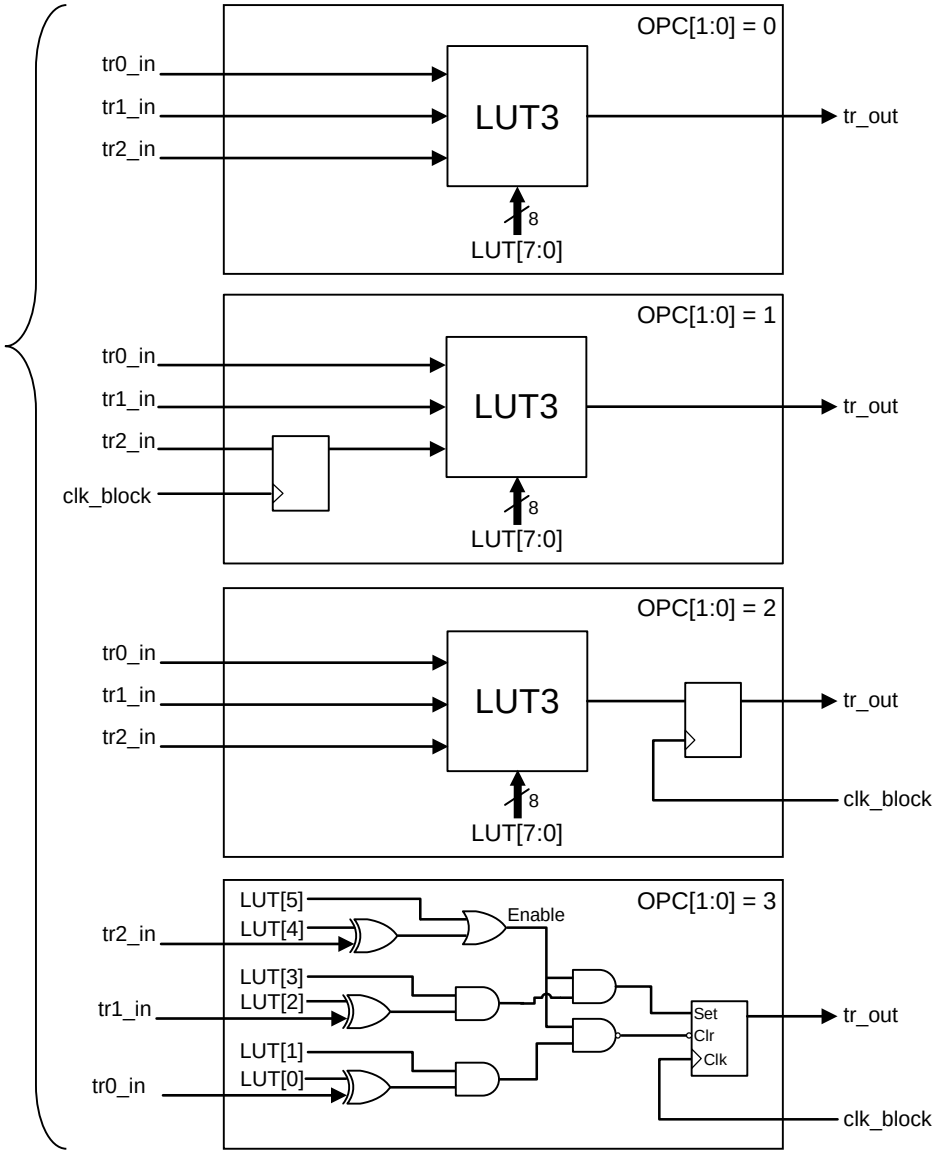
Review TRM section 22.12.2 and the Register TRM for additional details

Block Components (2/2)

- Three-input lookup table (LUT3)
  - Each Smart I/O block contains eight lookup table (LUT3) components
  - An LUT3 component consists of a three-input LUT and a flip-flop
  - OPC[1:0][1] determines the usage of flip-flop
  - LUT[7:0][2] is used as a lookup table for three input signals

tr2_in[2]	tr1_in[2]	tr0_in[2]	tr_out
0	0	0	LUT[0]
0	0	1	LUT[1]
0	1	0	LUT[2]
0	1	1	LUT[3]
1	0	0	LUT[4]
1	0	1	LUT[5]
1	1	0	LUT[6]
1	1	1	LUT[7]

[1] See the Register TRM (SMARTIO_LUT_CTL) for additional details
[2] Their inputs are defined by the SMARTIO_LUT_SEL register

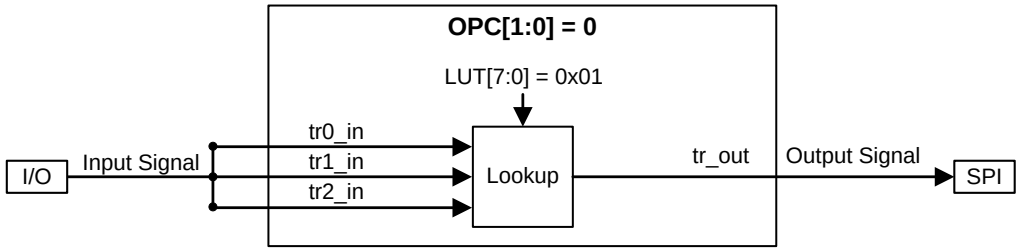


Hint Bar

Review TRM section 22.12.2 and the Register TRM for additional details

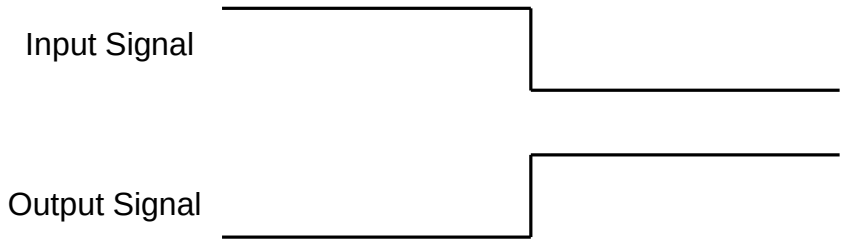
Use Case: Invert SPI Signal Polarity

› Use as an inverter by setting only OPC[1:0] = 0, LUT[7:0] = 0x01



LUT[7:0] = 0x01

tr2_in	tr1_in	tr0_in	tr_out
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

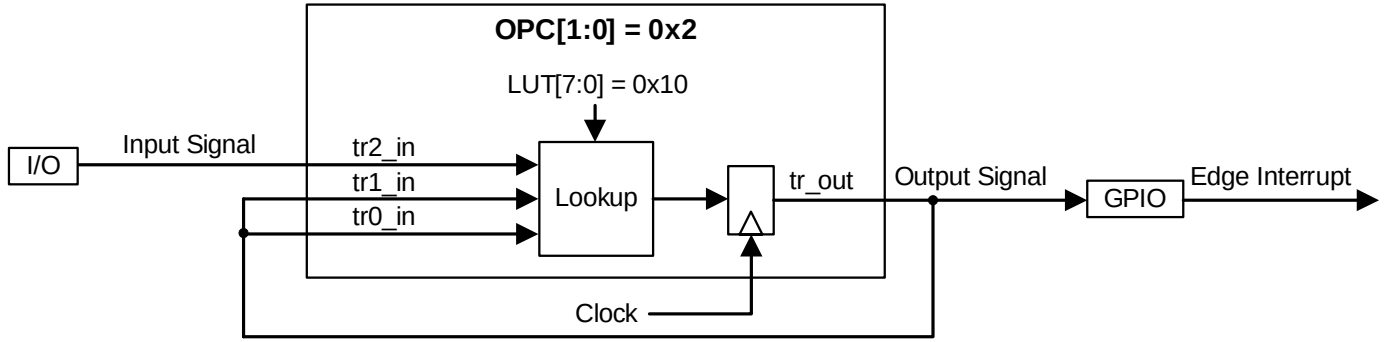


Hint Bar

Review TRM section 22.12.2 and the Register TRM for additional details

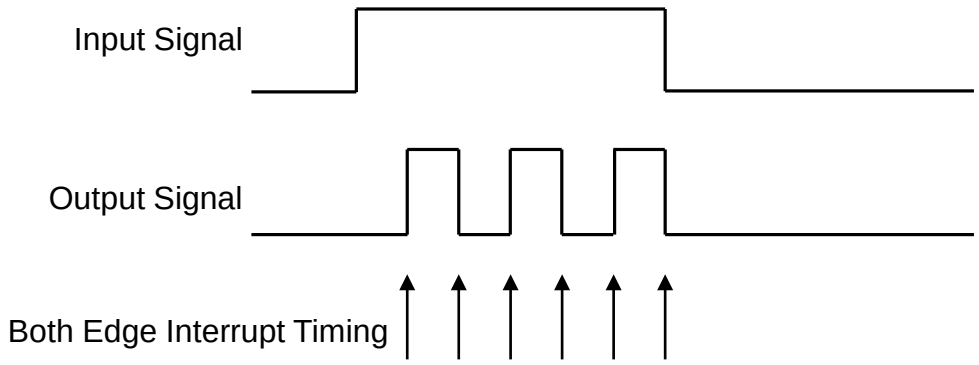
Use Case: High-Level Detection Interrupt

- Use as a high-level detection interrupt by using a GPIO edge interrupt and setting LUT3 to OPC[1:0] = 0x2, LUT[7:0] = 0x10



LUT[7:0] = 0x10

tr2_in	tr1_in	tr0_in	tr_out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

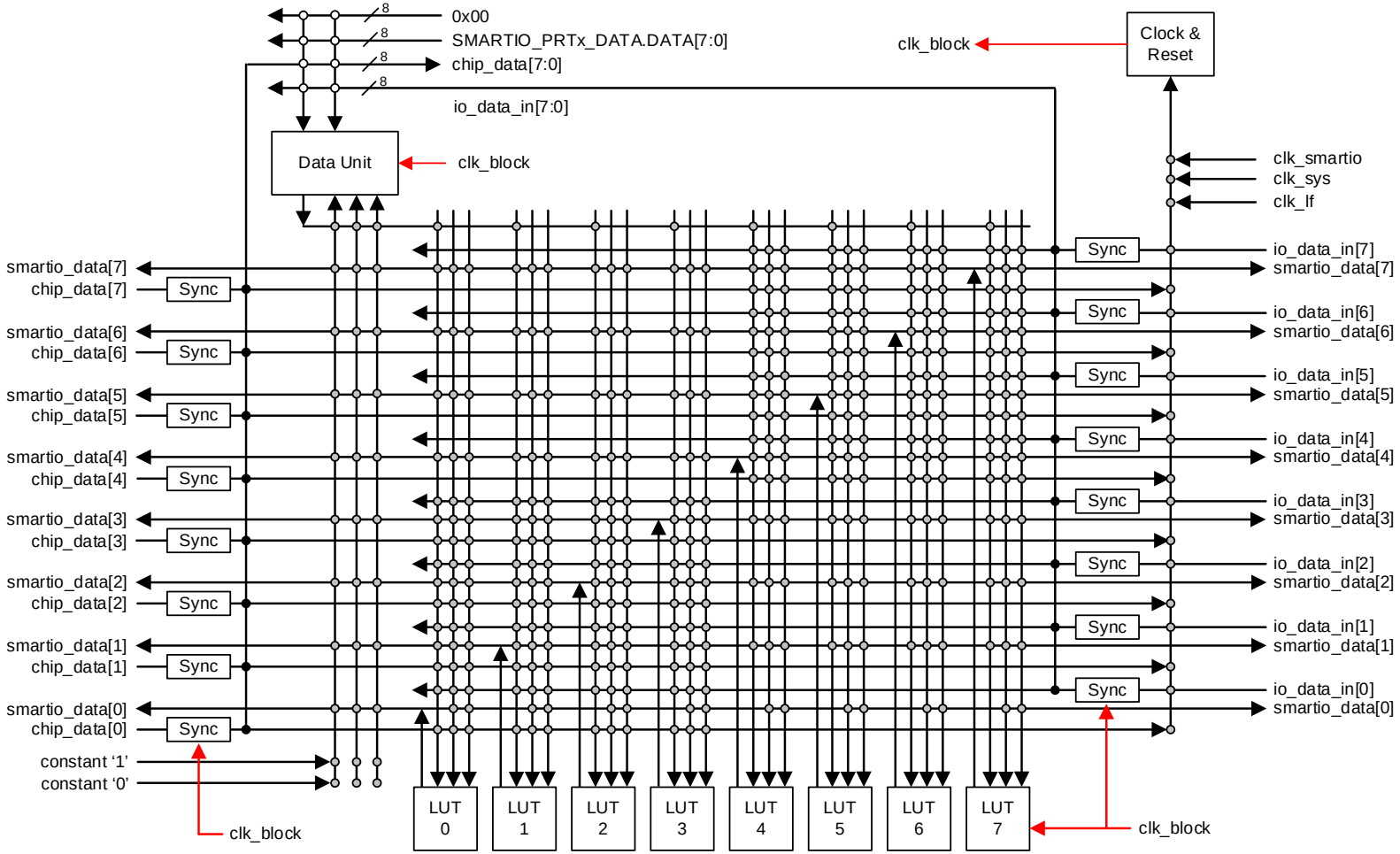


Hint Bar

Review TRM section 22.12.2 and the Register TRM for additional details

Routing

- Can be used to route signals in and out of the block and between various components inside the block



Hint Bar

Review TRM section 22.12.3 and the Register TRM for additional details

Additional reference material is available on web page at: Smart I/O Component Datasheet

Part of your life. Part of tomorrow.

Revision History

Revision	ECN	Submission Date	Description of Change
**	6172650	05/15/2018	Initial release
*A	6332068	10/04/2018	Added page 2, 4, 5, 14, and the note descriptions of all pages. Updated page 3, 11, 13, 15, 18, 20.
*B	6602988	06/25/2019	Added pages 5, 14, 16. Updated pages 2, 3, 4, 8, 9, 10, 11, 13, 15, 18.
*C	7024719	10/29/2020	Updated pages 2, 3, 12 to 18.
*D	7117273	04/05/2021	Updated pages 14, 16, 26 to 28.